CALL FOR PAPERS

UCAS-5

WORKSHOP on UNIQUE CHIPS and SYSTEMS

To be held in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2009)

April 26, 2009

Boston, Massachusetts, USA

Organizers:

Byeong Kil Lee, Texas Instruments Juan Rubio, IBM Austin Research Lab Dhireesha Kudithipudi, Rochester Institute of Technology

Program Committee:

Rajeev Balasubramonian, University of Utah Jeanine Cook, New Mexico State University Lee D. Coraor, Pennsylvania State University Manoj Franklin, University of Maryland Antonio Gentile, Università di Palermo, Italy

Eugene John, University of Texas at San Antonio Hyesoon Kim, Georgia Tech

Yong-Bin Kim, Northeastern University

Dhireesha Kudithipudi, Rochester Institute of Technology

Byeong Kil Lee, Texas Instruments

Hong Li, Intel

Tao Li, University of Florida

Kristina Lundqvist, Massachusetts Institute of Technology Rabi Mahapatra, Texas A&M University, College Station

Rama R. Menon, Intel Juan Rubio, ARL IBM

Zili Shao, The Hong Kong Polytechnic University Mohammad Tehranipoor, University of Connecticut

Jun Yang, University of Pittsburgh

Laurence T. Yang, St. Francis Xavier University, Canada Joshua Yi, Freescale

Important Dates:

Paper Submission:March2, 2009Notification of Acceptance:March30, 2009Final Version Due:April6, 2009

This workshop looks forward to bring together unique research in all areas of chip and system design. We are looking forward to assembling a program with unique technologies, circuits and architectures that your academic or industry team is working on.

Topics of interest include but not limited to unique aspects of:

- VLSI Systems
- Nanoelectronics and Gigascale Systems
- Software Systems
- Grid computing
- Pervasive Computing
- Radiation hardened systems
- Low Power Architectures and Systems
- Low Power Software
- Bioinformatics
- Integrated Security Systems
- Visualization
- Biometrics
- Biomedical
- Data hiding
- Blind Signal and Image Processing
- Wireless ad hoc and sensor networks
- Massively parallel architectures
- Multithreaded architectures
- Fine-grain parallel architectures
- Unique technologies (quantum well, optoelectronic, biologically inspired circuits/systems, RF and high frequency, etc)

Prospective authors are invited to submit a full paper not exceeding 8 pages in length in standard IEEE two-column format

For more information, visit the UCAS website at:

http://www.ispass.org/ucas5/