CALL FOR PAPERS

UCAS-6

The 6th INTERNATIONAL WORKSHOP on UNIQUE CHIPS and SYSTEMS

To be held in conjunction with MICRO-43

December 4, 2010
Atlanta, GA, USA

Organizers:

Byeong Kil Lee, *University of Texas at San Antonio*
Dhireesha Kudithipudi, *Rochester Institute of Technology*
Tor Aamodt, *University of British Columbia*

Program Committee:

Rajeev Balasubramonian, *University of Utah*
Pradip Bose, *IBM TJ Watson*
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Saraju Mohanty, *Univ. of North Texas*
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Sanghamitra Roy, *Utah State University*
Karu Sankaralingam, *University of Wisconsin*
Resit Sendag, *University of Rhode Island*
Michael Shebanow, *NVIDIA*
Lei Wang, *Univ. of Connecticut*

Important Dates:

Paper Submission:	Octoberber 3, 2010
Notification of Acceptance:	October 22, 2010
Final Version Due:	November 5, 2010

This workshop looks forward to bring together unique research in all areas of chip and system design. We are looking forward to assembling a program with unique technologies, circuits and architectures that your academic or industry team is working on.

UCAS-6 will have:
-Regular sessions (2 subcategories: computer architecture and VLSI)
-WIP (Work in Progress) session

Subcategories	**Topics of interest** include but not limited to unique aspects of:
I. Computer Architecture	• Massively parallel architectures • Multithreaded architectures • Fine-grain parallel architectures • Gigascale Systems • Software Systems • Grid computing • Mobile Cloud Computing • GPU / GPGPU • Performance Evaluation and Workload Characterization • Pervasive Computing • Low Power Software and Architectures
II. VLSI design	• Bioinformatics • Visualization • Biometrics / Biomedical • VLSI Systems • Nanoelectronics • Integrated Security Systems • Many-core architectures • Multimedia and Mobile processors • Unique technologies (quantum well, optoelectronic, biologically inspired circuits/systems,etc.) • Low Power Systems • Process Variation Tolerant Design
WIP (Work in Progress) session	The Work in Progress session is devoted to the presentation of new and on-going research in computer architecture and VLSI design. The primary purpose of the WIP session is to provide researchers with an opportunity to discuss their evolving ideas and get feedback in the workshop.

Submission Guideline: Prospective authors are invited to submit papers in standard IEEE two-column format:
-Regular sessions: ***not exceeding 8 pages (6~8 pages)***
-WIP (work-in-progress) session: ***4 pages***

For more information, visit the UCAS website at:
http://www.ispass.org/ucas6/