

# CALL FOR PAPERS

**HPCA-18** 

# The 7<sup>th</sup> INTERNATIONAL WORKSHOP on UNIQUE CHIPS and SYSTEMS

To be held in conjunction with HPCA-18

#### February 26, 2012 New Orleans, Louisiana, USA

## Organizers:

This workshop looks forward to bring together unique research in all areas of chip and system design. We are looking forward to assembling a program with unique technologies, circuits and architectures that your academic or industry team is working on.

Byeong Kil Lee, Univ of Texas at San Antonio Dhireesha Kudithipudi, RIT Tor Aamodt, University of British Columbia

### **Program Committee:**

Nak Woong Eum, ETRI Xin Fu, University of Kansas Paul Gratz, Texas A&M Univ, College Station Jie Han, University of Alberta Jaehyuk Huh, KAIST Ali Irturk, UCSD Canturk Isci, IBM TJ Watson Eugene John, UTSA Dimitris Kaseridis, ARM Tejas Karkhanis, IBM TJ Watson Omer Khan, Univ of Massachusetts Lowell Yong Bin Kim, Northeastern University Shigeru Kusakabe, Kyushu University Erik Lindholm, Nvidia Chen Liu. FIU Ingyu Lee, Troy University Mike O'Connor, AMD Resit Sendag, University of Rhode Island Michael Shebanow, Nvidia Abbas Sheibanyrad, TIMA Laboratory, France Lei Wang, University of Connecticut

UCAS-7 will have 2 main subcategories (computer architecture and VLSI design) and WIP (Work in Progress) session.

Subcategories	Topics of interest include but not limited to	
g	unique aspects of:	
I. Computer Architecture	<ul> <li>VLSI Systems</li> <li>Nanoelectronics and Gigascale Systems</li> <li>Software Systems</li> <li>Grid computing</li> <li>Mobile Cloud Computing</li> <li>GPU / GPGPU</li> <li>Pervasive Computing</li> <li>Radiation hardened systems</li> <li>Low Power Architectures and Systems</li> <li>Low Power Software</li> <li>Bioinformatics</li> <li>Integrated Security Systems</li> <li>Visualization</li> <li>Biometrics / Biomedical</li> <li>Data hiding</li> </ul>	
II. VLSI design	<ul> <li>Bind Signal and Image Processing</li> <li>Wireless ad hoc and sensor networks</li> <li>Massively parallel architectures</li> <li>Multithreaded architectures</li> <li>Fine-grain parallel architectures</li> <li>Many-core architectures</li> <li>Multimedia and Mobile processors</li> <li>Performance Evaluation and Workload Characterization</li> <li>Unique technologies (quantum well, optoelectronic, biologically inspired circuits/systems, RF and high frequency, etc.)</li> </ul>	
WIP (Work in Progress) session	The Work in Progress session is devoted to the presentation of new and on-going research in computer architecture and VLSI design. The primary purpose of the WIP session is to provide researchers with an opportunity to discuss their evolving ideas and get feedback in the workshop.	

#### Important Dates: Paper Submission: December 16, 2011

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Notification of Acceptance:	January 16, 2012
Final Version Due:	January 23, 2012

**Submission Guideline:** Prospective authors are invited to submit a full paper *not exceeding 8 pages (6~8 pages)* in length in standard IEEE two-column format for regular sessions; *4 pages* in length in standard IEEE two-column format for WIP session.

Submission site: http://chicago.ece.utsa.edu/ucas7

For more information, visit the UCAS website at:

http://www.ispass.org/ucas