Sunday, November 4:

10:00 AM-11:30 AM: Tutorial I
Tutorial Session Chair: Kathy Kackson, IBM
Power-Efficient Architectures: Trends, Metrics and Modeling Challenges
David Brooks, Viji Srinivasan, Pradip Bose, Philip Emma (IBM T. J. Watson Research Center), presented by Pradip Bose

11:30-2:00 PM: Lunch Break
Lunch sponsored by virtutech

2:00 PM-5:30 PM: Tutorial II
Tutorial Session Chair: Kathy Kackson, IBM
Simics—A fast, multi-target, portable, full system simulator
Peter Magnusson (virtutech)

Monday, November 5:

7:30 AM-9:00 AM: Registration

9:00 AM-9:15 AM: Welcome and Introduction of Keynote Speaker

9:15 AM-10:15 AM: Keynote Address

EV8: Design, Modeling and Little's Law
Dr. Joel Emer (Intel Corp.)

10:15 AM-10:40 AM: Coffee Break

10:40 AM-12:00 PM: Session 1: Processor-Level Modeling and Analysis
Session Chair: Craig Chase, U of Texas at Austin
MASE: A novel infrastructure for detailed microarchitectural modeling
Eric Larson, Saugata Chatterjee, Todd Austin (University of Michigan)
Early design stage power-performance modeling through statistical simulation
Lieven Eeckhout, Koen De Bosschere (Ghent University, Belgium)
Performance analysis using pipeline visualization
Chris Weaver, Kenneth C. Barr, Eric D. Marsman, Dan Ernst, Todd Austin (University of Michigan)

12:00 PM-2:00 PM: Lunch Break
Lunch sponsored by ISPASS

12:00 PM-12:30 PM: Invited Luncheon Speaker
Valerie Taylor (Northwestern University)
Prophesy: Automating the Modeling Process
Valerie Taylor, Xingfu Wu, Jonathan Geisler, Xin Li, Zhiling Lan, Mark Hereld, Ivan Judson, Rick Stevens (Northwestern University)

2:00 PM-3:50 PM: Session 2: Software (OS) Performance Analysis
Session Chair: Peter Magnusson, virtutech
Implementation and evaluation of a best-effort scheduling algorithm in an embedded real-time system
Peng Li, Binoy Ravindran, Tamir Hegazy (Virginia Polytechnic Institute and State University)
An evaluation of POSIX trace standard implemented in RT-Linux
Andrés Terrasa, Ignacio Pachès, Ana García-Fornes (Universidad Politécnica de Valencia, Spain)
A cycle-accurate per-thread timer for Linux operating system
Yang Qian, Witawas Srisa-an, Therapon Skonitiotis, J. Morris Chang (Illinois Institute of Technology)

3:50 PM-4:15 PM: Coffee Break

Session Chair: Nasr Ullah, Motorola
Geist: A generator of E-Commerce and Internet server traffic
Krishna Kant, Vijay Tewari, Ravi Iyer (Intel Corporation)
Performance characterization of multi-tier E-Business systems using queueing operational systems
Deep K. Buch, Vladimir M. Pentkovski (Intel Corporation)

6:00 PM: Conference Reception
Drinks and Hors d’oeuvres
Tuesday, November 6:

8:00 AM-9:00 AM: **Session 4: Control-Flow Characterization**
Session Chair: Manoj Franklin, U of Maryland
Understanding the control flow transfer and its predictability in Java Processing
Tao Li, Lizy Kurian John *(University of Texas at Austin)*

The effects of context switching on branch predictor performance
Michele Co, Kevin Skadron *(University of Virginia)*

9:00 AM-9:30 AM: **Coffee Break**

9:30 AM-11:00 AM: **Session 5: Memory Characterization I**
Session Chair: Kathy Jackson, IBM
Evaluating internal memory fragmentation for Java programs
Therapon Skotiniotis, J. Morris Chang *(Illinois Institute of Technology)*

An evaluation of search tree techniques in the presence of caches
Costin Iancu, Anurag Acharya *(University of California, Santa Barbara)*

Automatic memory hierarchy characterization
Clark L. Coleman, Jack W. Davidson *(University of Virginia)*

11:00 AM-11:10 AM: **Break**

11:10 AM-12:00 PM: **Session 6: Memory Characterization II**
Session Chair: Kathy Jackson, IBM
Increasing file prediction accuracy with program- and user-based last successors
Tsozen Yeh, Darrell D. E. Long, Scott A. Brandt *(University of California, Santa Cruz)*

Efficient profile-based evaluation of randomising set index functions for cache memories
Hans Vandierendonck, Koen De Bosschere *(Ghent University, Belgium)*

12:00 PM-2 PM: **Lunch Break**
Lunch sponsored by ISPASS

12:00 PM-12:30 PM: **Invited Luncheon Speaker**
Frederica Darema *(NSF/CISE)*
Performance Engineering Projects funded under the NSF Next Generation Software (NGS) Program

2:00 PM-3:20 PM: **Session 7: Systems and Servers**
Session Chair: Frederica Darema, NSF
Workload characterization of multithreaded Java servers
Yue Luo, Lizy Kurian John *(University of Texas at Austin)*

Behavior and performance/scalability of interactive multiplayer internet game servers
Ahmed Abdelkhaelek, Angelos Bilas, Andreas Moshovos *(University of Toronto)*

Parallel simulation of multiprocessor execution: implementation and results for simplescalar
Naraig Manjikian *(Queen's University, Kingston, Ontario)*

3:20 PM-3:40 PM: **Coffee Break**

3:40 PM-4:30 PM: **Session 8: Scheduling and Verification**
Session Chair: Todd Austin, U of Michigan
Locality-aware predictive scheduling of network processors
Tilman Wolf, Mark A. Franklin *(Washington University in St. Louis)*

Statistical usage testing applied to mobile network verification
Alexander Ost, Dorien van Logchem *(Ericson Eurolab, Germany)*

4:30 PM-5:50 PM: **Session 9: Advanced Microarchitectures and their Evaluation**
Session Chair: Pradip Bose, IBM
Balancing throughput and fairness in SMT processors
Kun Luo, Jayanth Gummaraju, Manoj Franklin *(University of Maryland)*

An empirical study of the scalability aspects of instruction distribution algorithms for clustered processors
Aneesh Aggarwal, Manoj Franklin *(University of Maryland)*

5:50 PM: **Closing Remarks**

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How to compare the performance of two SMT microarchitectures
Yiannakis Sazeides *(University of Cyprus)*, Toni Juan *(Universitat Politècnica de Catalunya)*

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